In the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-7. (Canceled)

8-13. (Canceled).

14. (Previously presented) An interconnect structure, comprising:

a substrate;

a plurality of first metal lines disposed on the substrate;

a first insulating layer disposed on the substrate, covering the plurality of first metal lines;

a plurality of second metal lines disposed on the first insulating layer;

a second insulating layer covering the plurality of second metal lines;

a plurality of ITO (indium tin oxide) wirings, each ITO wiring electrically connecting one of the plurality of first metal lines and one of the second metal lines respectively;

a passivation structure disposed on the second insulating layer, wherein the passivation structure comprises a plurality of openings, wherein each of the opening exposes only one of corresponding ITO wirings, and each of the openings is separated from the adjacent opening by a surrounding wall; and

a plurality of residue ITO rings remains along inner foots of the openings, wherein the residue ITO rings do not extend beyond the openings.

15. (Previously presented) The interconnect structure as claimed in claim 14, wherein the substrate is a TFT-array substrate for a flat display panel.

16. (Previously presented) The interconnect structure as claimed in claim 14, wherein the plurality of first and second metal lines, the plurality of ITO wirings and the passivation structure are disposed in a non-display area of the TFT-array substrate.

17. (Previously presented) The interconnect structure as claimed in claim 16, wherein the plurality of first metal lines are gate metal lines formed simultaneously with gate metal lines in a display area of the TFT-array substrate.

18. (Previously presented) The interconnect structure as claimed in claim 17, wherein the plurality of second metal lines are source/drain metal lines that are formed simultaneously with source/drain metal lines on a display area of the TFT-array substrate.

19. (Previously presented) The interconnect structure as claimed in claim 14, wherein each of the ITO wirings comprises a first ITO electrode disposed in the first and second insulating layers in contact with each of the first metal lines, a second ITO electrode disposed in the second insulating layer in contact with each of the second metal lines, and an ITO layer connecting the first and second ITO electrodes.